REMARKS

Claims 1-88 were presented for examination and were pending in this application. Claims 1-36 and 79-88 were previously withdrawn.

Applicants thank the Examiner for examination of the claims pending in this application.

Applicants herein amend claims 37, 43, 46, 49, 52-53, 56-57, 59, 64, 67-68, 70 and 74. New claim 89 has been added. These changes are believed not to introduce new matter, and their entry is respectfully requested. In making these amendments, Applicants do not concede that the subject matter of such claims was in fact disclosed or taught by the cited prior art. Rather, Applicants reserve the right to pursue such protection at a later point in time and merely seeks to pursue protection for the subject matter presented in this submission.

Based on the above Amendment and the following Remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections, and withdraw them.

Response to Claim Objections

On page 2 of the Office Action, the Examiner objected to typographical errors in claims 49 and 67. Applicants have amended these claims to correct such errors or to provide clarification. Applicants accordingly respectfully request that the Examiner withdraw the corresponding objections.

Response to Claim Rejections Under 35 USC 102(b)

On page 3 of the Office Action, the Examiner rejected independent claim 52 under 35 U.S.C. §102(b) as being anticipated by Rompaey (E.U. Application 96870126.8). This rejection is respectfully traversed.

Amended claim 52 recites a computer implemented method of embedded system design, comprising:

> ...
>
> generating ... a finite state machine (FSM) representation of at least one hardware component, said generating comprising applying a design language having at least one graphical symbol and adapted to form an FSM representation of electronic hardware, each graphical symbol of the design language having a graphical portion and a... textual portion...
>
> ...
>
> creating a virtual test bench using a test bench builder for generating a graphical representation of at least one interactive test bench and for selecting signals or variables to be coupled to a graphical representation of a user interface for each interactive test bench;
>
> ...

The claimed invention thus provides a design method that comprises at least i) building an FSM representation of a hardware component using a graphical design language, and ii) applying a test bench builder to create an interactive virtual test bench having selected signals or variables coupled to a graphical user interface.

The claimed invention is patentably distinguishable over Rompaey. Rompaey discloses a design environment and method for implementing a heterogeneous essentially digital system. (Rompaey, Abstract) The design environment and method of Rompaey are based on encapsulation of existing hardware and software compilers and allow interactive synthesis of hardware/software and hardware / hardware interfaces. (Rompaey, Summary of the Invention) However, Rompaey fails to disclose or suggest a design method that comprises at least elements i) and ii) of the claimed invention as described above. Thus, Applicants respectfully

submit that for at least this reason amended claim 52 is patentably distinguishable over Rompaey. Therefore, Applicants respectfully request that the Examiner reconsider the rejection and withdraw it.

Dependent claims 53-63 depend directly or indirectly from claim 52 and recite additional patentable features. For example, claim 56 recites the step of loading benchmark software in an evaluation phase of an embedded system project and running a simulation of the virtual embedded system executing the benchmark software. Applicants respectfully submit that claims 53-63 are also distinguishable over the cited reference. Therefore, Applicants respectfully request that the Examiner reconsider the corresponding rejections and withdraw them.

On page 5 of the Office Action, the Examiner rejected claim 64 under 35 U.S.C. §102(b) as being anticipated by Rompaey. This rejection is respectfully traversed. Amended claim 64 recites a method of designing an embedded system, the method comprising:

> ...
>
> generating a[n]... FSM... representation of at least one hardware element, said generating comprising applying a design language having at least one graphical symbol and adapted to form a finite state machine representation of electronic hardware, each graphical symbol of the design language having a graphical portion and a... textual portion...
>
> ...
>
> creating a virtual test bench having a graphical representation of a human/machine interface for interacting with the embedded system using a test bench builder for generating a graphical representation of at least one interactive test bench and for selecting signals or variables associated with the FSM and to be coupled to a graphical representation of a user interface for each interactive test bench;
>
> ...

The claimed invention thus provides a method of designing an embedded system that comprises i) and ii) as described above in connection with amended claim 52. Thus, Applicants respectfully submit that for at least the reason discussed above with respect to amended claim 52,

amended claim 64 is patentably distinguishable over Rompaey. Therefore, Applicants respectfully request that the Examiner reconsider the rejection and withdraw it.

Dependent claims 65-67 depend directly or indirectly from claim 64 and recite additional patentable features. For example, claim 65 recites the step of developing a hardware implementation using the virtual prototype as a functional specification describing a hardware partition. Applicants respectfully submit that claims 65-67 are also distinguishable over the cited reference. Therefore, Applicants respectfully request that the Examiner reconsider the corresponding rejections and withdraw them.

New claim 89 depends from claim 64 and recites the step of interacting at run-time with the virtual prototype to simulate an application of the embedded system. Applicants submit that claim 89 is also distinguishable over the cited reference, and respectfully request that this claim be allowed.

Response to Claim Rejections Under 35 USC 103(a)

On page 6 of the Office Action, the Examiner rejected claim 37 under 35 U.S.C. §103(a) as being unpatentable over Rompaey in view of Hellestrand et al. (U.S. patent no. 6,263,302). This rejection is respectfully traversed. Amended claim 37 recites a method of designing an embedded system, the method comprising:

> ...forming a virtual embedded system including an instruction set accurate simulator... coupling read, write, and interrupt signals of the instruction set accurate simulator with an FSM simulation of at least one hardware element, wherein generating said FSM simulation comprises applying a design language having at least one graphical symbol and adapted to form a finite state machine representation of electronic hardware, each graphical symbol of the design language having a graphical portion and a user-definable textual portion defining the behavior of the graphical symbol;

> ...displaying on the GUI... a virtual test-bench associated with the GUI and adapted to interact with the simulation, wherein the virtual test-bench is created using a test-bench builder for generating a graphical representation of at least one interactive test-bench and for selecting signals or variables associated with the FSM and to be coupled to a graphical... user interface for each interactive test-bench, to emulate user input to and device output from the virtual embedded system.

The claimed invention thus provides a method of designing an embedded system that comprises at least i) and ii) as described above in connection with amended claim 52. Thus, Applicants respectfully submit that for at least the reason discussed above with respect to amended claim 52, amended claim 37 is patentably distinguishable over Rompaey.

Hellestrand does not remedy the shortcomings of Rompaey. Hellestrand discloses a co-simulation design system that runs on a host computer and includes a hardware simulator and a processor simulator coupled via an interface mechanism. The processor simulator provides accurate timing information whenever the processor simulator interacts with the hardware simulator. (Hellestrand, Abstract) Hellestrand, however, also fails to disclose at least a design method that comprises elements i) and ii) of the claimed invention as described above in connection with claim 52. Thus, Applicants respectfully submit that for at least this reason, a prima facie case of obviousness has not been established, and therefore that amended claim 37 is patentably distinguishable over the combination of Rompaey and Hellestrand. Therefore, Applicants respectfully request that the Examiner reconsider the rejection and withdraw it.

Dependent claims 38-51 depend directly or indirectly from claim 37 and recite additional patentable features. For example, claim 38 recites that the design language includes a plurality of graphical symbols with each graphical symbol having a graphical semantic portion and a textual semantic portion. Applicants respectfully submit that claims 38-51 are also distinguishable over the cited references. Therefore, Applicants respectfully request that the Examiner reconsider the corresponding rejections and withdraw them.

On page 14 of the Office Action, the Examiner rejected claim 68 under 35 U.S.C. §103(a) as being unpatentable over Rompaey in view of Van Huben et al. (U.S. patent no. 6,094,654). This rejection is respectfully traversed. Amended claim 68 recites a method of providing information to potential suppliers for procuring a good or service associated with an embedded system, the method comprising:

...

> designing a... virtual prototype having an instruction set accurate simulator of a target processor core and a[n]... FSM representation..., wherein generating said FSM representation comprises applying a design language having at least one graphical symbol and adapted to form a finite state machine representation of electronic hardware, each graphical symbol of the design language having a graphical portion and a user-definable textual portion defining the behavior of the graphical symbol;
>
> creating a virtual test bench having a graphical representation of a human/machine interface for interacting with the embedded system using a test bench builder for generating a graphical representation of at least one interactive test bench and for selecting signals or variables associated with the FSM and to be coupled to a graphical representation of a user interface for each interactive test bench;

...

The claimed invention thus provides a method of designing an embedded system that comprises at least i) and ii) as described above in connection with amended claim 52. Thus, Applicants respectfully submit that for at least the reason discussed above with respect to amended claim 52, amended claim 68 is patentably distinguishable over Rompaey.

Van Huben does not remedy the shortcomings of Rompaey. Van Huben discloses a design control system suitable for use in connection with the design of elements of manufacture which need to be developed in a concurrent engineering environment. A model is created and/or identified by control information, and design libraries hold pieces of the design under control of the system. (Van Huben, Abstract). However, Van Huben also fails to disclose at least a design method that comprises elements i) and ii) of the claimed invention as described above in connection with claim 52. Thus, Applicants respectfully submit that for at least this reason, a

prima facie case of obviousness has not been established, and therefore that amended claim 68 is patentably distinguishable over the combination of Rompaey and Van Huben. Therefore, Applicants respectfully request that the Examiner reconsider the rejection and withdraw it.

Dependent claims 69-73 depend directly or indirectly from claim 68 and recite additional patentable features. For example, claim 69 recites that the virtual prototype is stored on a computer readable medium and that publishing the virtual prototype comprises sending the computer readable medium to a vendor. Applicants respectfully submit that claims 69-73 are also distinguishable over the cited references. Therefore, Applicants respectfully request that the Examiner reconsider the corresponding rejections and withdraw them.

On page 16 of the Office Action, the Examiner rejected claim 74 under 35 U.S.C. §103(a) as being unpatentable over Van Huben in view of Rompaey. This rejection is respectfully traversed. Amended claim 74 discloses a computer-implemented method for a vendor to acquire information for the procurement of a good or service related to an embedded system project, the method comprising:

> accessing a database of virtual prototypes of embedded systems, each of the virtual prototypes having... a[n] FSM... representation of hardware peripherals, and a virtual test bench emulating a human/machine interface for interacting with a simulation of the operation of the virtual prototype,
>
> wherein generating said FSM representation comprises applying a design language having at least one graphical symbol and adapted to form a finite state machine representation of electronic hardware, each graphical symbol of the design language having a graphical portion and a user-definable textual portion defining the behavior of the graphical symbol, and
>
> wherein the virtual test bench is created using a test bench builder for generating a graphical representation of at least one interactive test bench and for selecting signals or variables associated with the FSM and to be coupled to a graphical representation of a user interface for the interactive test bench;
>
> ...

The claimed invention thus provides a method for a vendor to acquire information for the procurement of a good or service, the method comprising at least i) and ii) as described above in connection with amended claim 68. Thus, Applicants respectfully submit that for at least the reason discussed above with respect to amended claim 68, amended claim 74 is patentably distinguishable over the combination of Van Huben and Rompaey. Therefore, Applicants respectfully request that the Examiner reconsider the rejection and withdraw it.

Dependent claims 75-78 depend directly or indirectly from claim 74 and recite additional patentable features. For example, claim 75 recites the step of submitting a quote for a good or service related to the embedded system simulated by the virtual prototype. Applicants respectfully submit that claims 75-78 are also distinguishable over the cited references. Therefore, Applicants respectfully request that the Examiner reconsider the corresponding rejections and withdraw them.

Conclusion

Applicants respectfully submit that claims 37-78 and 89, as presented herein, are patentably distinguishable over the cited references. Therefore, Applicants request reconsideration and allowance of these claims.

In addition, Applicants respectfully invite the Examiner to contact Applicants' representative at the number provided below if the Examiner believes it will help expedite furtherance of this application.

RESPECTFULLY SUBMITTED,
STEPHEN BADE, ET AL.

Date: MAY 15, 2006 By: David K. Varn

David K. Varn, Reg. No. 53,718
FENWICK & WEST LLP
Silicon Valley Center
801 California Street
Mountain View, CA 94041
Phone: (650) 335-7183
Fax: (650) 938-5200